AD5522 DATA SHEET SPECIFICATION AND TIMING REVISION COMPARISON

SPECIFICATION	PAGE #	REV. E	REV F.
FORCE CURRENT, Voltage Compliance, EXTFOHx2	7	AVSS+4; AVDD-4	AVSS+6; AVDD-3
FORCE CURRENT, Voltage Compliance, EXTFOHx2, Comments	7		"Supports 64 mA sink current, 80 mA source current"
FORCE CURRENT, New Line, Voltage Compliance, EXTFOHx2, Comments	7		"Supports 80 mA sink and source current"
FORCE CURRENT, Force Current Ranges	7	Max +/-80mA	Typical +/-64 ; Max +/-80mA
FORCE CURRENT, Force Current Ranges, Comments	7	"Set using external sense resistor; internal amplifier can drive up to ±80 mA"	Set using external sense resistor; internal amplifier can drive up to ±80 mA with increased compliance.
Timing Characteristics, "t16" omitted	12	1.8,1.2,0.9	
Timing Characteristics, New "t16A"	12		4.0, 4.0, 4.0, Description, RESET pulse width low min
Timing Characteristics, New "t16B"	12		4.0, 4.0, 4.0, µs max, RESET low to BUSY low max
Timing Characteristics, "t17"	12	670, 700,750	750, 750, 750
CHOSSING POWER SUPPLY RAILS, after "Iload is the maximum load current."	33		Also consideration to power supply headroom and footroom is required to achieve full output current in both the internal and external current ranges as shown in the FORCE CURRENT section of the Specification section. For example, to achieve the full 80mA sink capability, the foot room needs to increase from AVSS+3V to AVSS+6V."
Table 10, NEW footnote 2	33		^2 VMID = 3.5 × VREF × ((42,130 - OFFSET_DAC_CODE)/216) as specified on Page 32.
Table 11, Transfer Function, MV	33	0.2 × (VDUT × VREF × OFFSET_DAC_CODE/2^16)	0.2 × ((VDUT -DUTGND) – VMIN^3)
Table 11, NEW footnote 3	33		VMIN = -3.5 × VREF × (OFFSET_DAC_CODE/216) as specified on Page 32.

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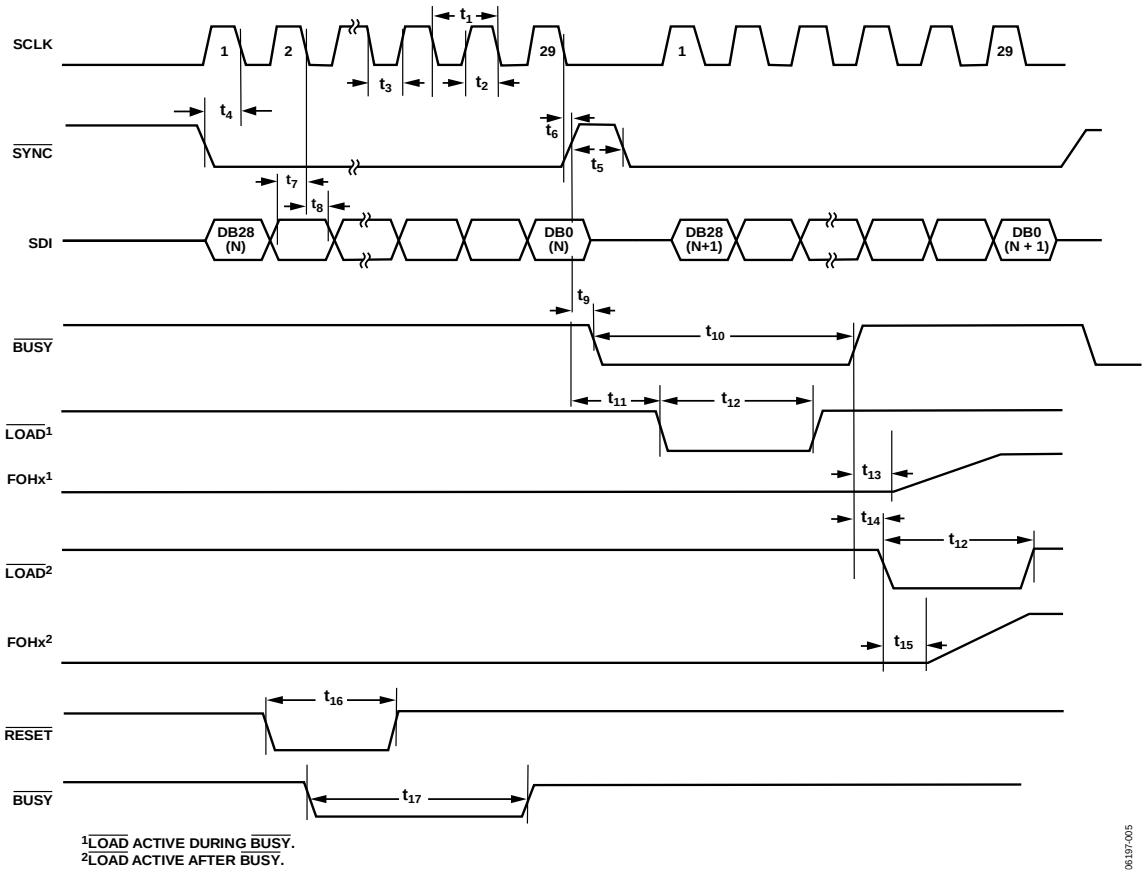
SPECIFICATION	PAGE#		
Figure 5	13		

REV. E



1LOAD ACTIVE DURING BUSY.
2LOAD ACTIVE AFTER BUSY.

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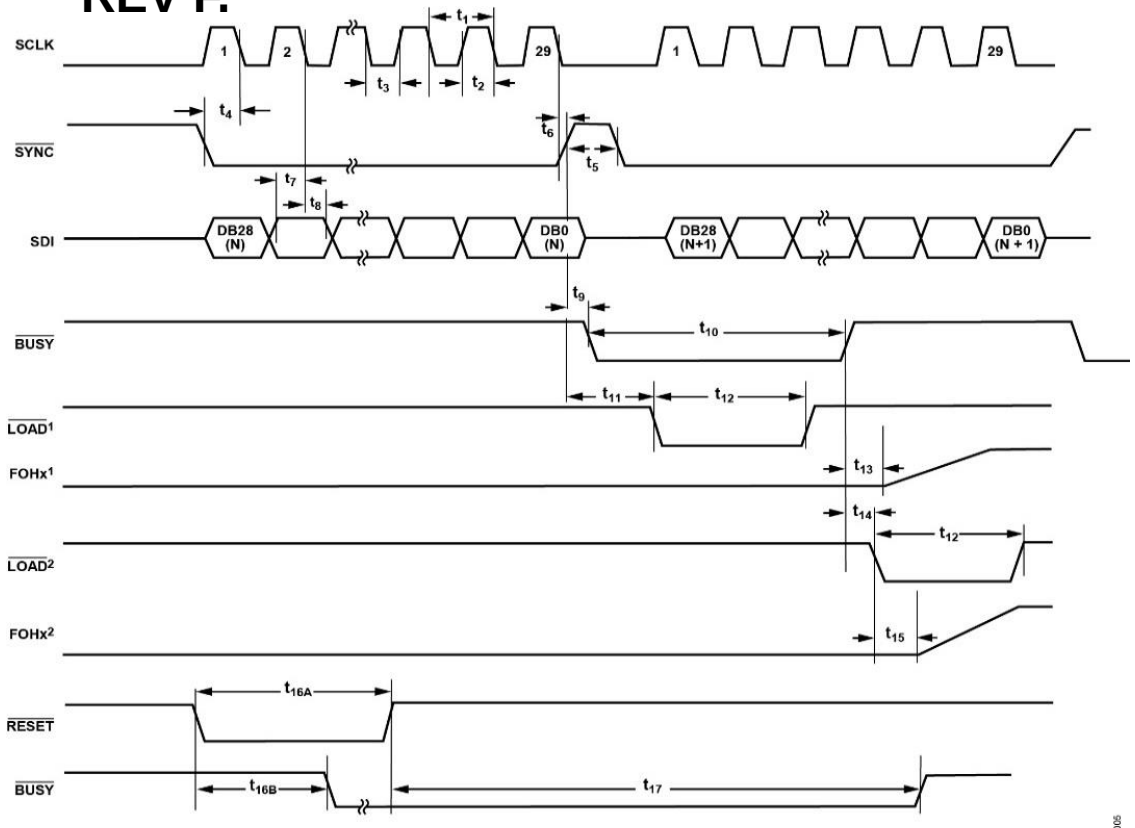
REV F.



1LOAD ACTIVE DURING BUSY.
2LOAD ACTIVE AFTER BUSY.

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